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*Q. 4.1: Consider the  
combinational circuit shown  
in Fig. P4.1. (a) \* Derive the  
Boolean expressions fo  $\phi$ .*

~~4.7: Design a combinational~~

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~~circuit that converts a four-bit Gray code (Table 1.6) to a bit four Q. 4.26:~~

~~Construct a 4-to-16-line decoder with five~~

~~2-to-4-line decoders with enable. Q. 4.23: Draw the~~

~~logic diagram of 2-to-4-line~~

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*decoder using (a) NOR gates  
only (b) NAND gates only*

**Design of 4 × 4 RAM ||**

**Construction of a 4 × 4 RAM**

**|| RAM in computer**

**architecture | 4\*4 RAM**

**design Q. 4.3: For the**

**circuit shown in Fig. 4.33**



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(Section 4.11), (a) Write the  
Boolean functions Q. 1.1:

List the octal and  
hexadecimal numbers from 16  
to 32. Using A and B for the  
last two digits Q.

*4.8: Design a code converter  
that converts a decimal*

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digit from the 8, 4, -2, -1  
code to BCD Q. 3.29:

Implement the following four  
Boolean expressions with  
three half adders:  $D = A \oplus B \oplus C$

Q. 4.4: Design a  
combinational circuit with  
three inputs and one

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output. (a) The output is 1  
when Q. 6.7: Draw the logic  
diagram of a four-bit  
register with four D  
flip-flops and four  $4 \times 1$   
multiple Learn how to create  
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What Is Digital Design? -

~~Deepend Implement boolean  
function using decoder~~ **state**

**diagram/state table/circuit**

**diagram (using D-flip flop)**

**- Digital Logic Design**

*Combinational circuit with*

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*decoder and external logic  
gates - Digital Electronics*

*Example Lesson 11 - VHDL*

*Example 3: Majority Circuit*

---

*Lesson 14 - PLDs and CPLDs*

*Sequential Circuit Analysis  
- From sequential circuit to  
state transition diagrams.*

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*Brilliantly Animated Annual  
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InDesign \u0026 in5 Q. 5.10:*

A sequential circuit has two JK flip-flops A and B, two inputs x and y, and one output z

---

Lecture 4: Digital Logic

*Page 14/52*

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م. ی. م. ص. ت. ی. ب. ر. ع. ل. ا. ب. ح. ر. ش. ق. ط. ن. م. ل. ا.  
Q. ق. ط. ن. م. ل. ا. ر. ئ. ا. و. د. ح. ر. ش. - ق. ط. ن. م. ل. ا.

5.6: A sequential circuit with two D flip-flops A and B, two inputs, x and y; and one output z is **Q. 5.1: The D latch of Fig. 5.6 is constructed with four NAND**

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gates and an inverter.

**Consider the** *Digital Logic  
Design - Unit 04 -*

*Combinational Logic - Part  
03 - Design Procedure Q.*

3.6: Simplify the following  
Boolean expressions, using  
four-variable maps: (a)



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A'B'C'D' + AC'D' + Q. 4.37:

Implement the following  
Boolean function with a 4 \* 1

multiplexer and external

gates **Q. 4.35: Implement a**

**full adder with two 4 \* 1**

**multiplexers.** ~~Digital Design~~

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